AMENDMENTS

IN THE CLAIMS:

Please cancel claims 1-7, and add new claims 11-26 as follows below.

Claims 1-7 (Cancelled).

Claim 8 (Original): A method for forming a LDMOS transistor, comprising:

forming an epitaxial layer on a semiconductor substrate;

forming a deep n-well region in said epitaxial layer;

forming a patterned photoresist layer over said deep n-well region wherein said patterned photoresist layer comprises at least one opening;

implanting a boron species into said deep n-well through said opening;

performing a hard bake process on said patterned photoresist layer;

implanting an arsenic species into said deep n-well through said opening;

forming LOCOS isolation structures in said deep n-well region; and

forming a gate dielectric layer on said deep n-well region.

Claim 9 (Original): The method of claim 8 wherein said hard bake process comprises heating said patterned photoresist layer to a temperature between 75° C and 200° C.

Claim 10 (Original): The method of claim 9 wherein forming said LOCOS isolation structures comprises performing thermal oxidation processes at temperatures greater than 800° C.

Claim 11 (New): The method of claim 8 wherein implanting the boron species into said deep n-well through said opening comprises implanting the boron species at two or more implantation energies and dose levels through said opening.

Claim 12 (New): The method of claim 8 wherein the hard bake process on said patterned photoresist layer is performed after implanting the boron species into the deep n-well region.

Claim 13 (New): The method of claim 8 wherein the implanting of the arsenic species into the deep n-well is performed after the hard bake into said deep n-well through said opening.

Claim 14 (New): The method of claim 8 wherein the forming of the LOCOS isolation structures in said deep n-well region is performed after implanting the arsenic species into a source region in the deep n-well.

Claim 15 (New): A method for forming a LDMOS transistor, comprising:

forming a deep n-well region in an epitaxial layer of a semiconductor substrate;

forming a patterned photoresist layer over said deep n-well region wherein said patterned photoresist layer comprises an opening overlying a source region in the deep n-well region;

implanting a boron species at a first implantation energy and dose into the source region through said opening;

performing a hard bake process on said patterned photoresist layer after implanting the boron species into the source region;

implanting an arsenic species after the hard bake into the source region through said opening; and

performing a thermal annealing cycle on the transistor after implanting the arsenic species into the source region, wherein a diffusion of the boron and arsenic species results thereby.

Claim 16 (New): The method of claim 15 wherein said hard bake comprises heating said patterned photoresist layer to a temperature between 75° C and 200° C.

Claim 17 (New): The method of claim 15 wherein the first boron implantation energy and dose comprises an energy of about 300KeV to about 500KeV and a dose of about 5xE13cm-2 to about 5xE14cm-2.

Claim 18 (New): The method of claim 17 further comprising a second boron implantation into the source region through said opening the second implantation energy and dose comprising an energy of about 40KeV to about 60KeV and a dose of about 5xE12cm-2 to about 5xE13cm-2.

Claim 19 (New): The method of claim 15 wherein said thermal annealing cycle occurs at a temperature between 800° C and 1200° C.

Claim 20 (New): The method of claim 15 further comprising forming a gate dielectric layer overlying said deep n-well region.

Claim 21 (New): A method for forming a LDMOS transistor, comprising:

forming a deep n-well region in an epitaxial layer of a semiconductor substrate;

forming a patterned photoresist layer over said deep n-well region wherein said patterned photoresist layer comprises an opening overlying a source region in the deep n-well region;

implanting a first species at a first and second implantation energy and dose into the source region through said opening;

performing a hard bake process on said patterned photoresist layer after implanting the first species into the source region;

implanting a second species of opposite polarity than the first species into the source region through said opening after the hard bake; and

performing a thermal annealing cycle on the transistor after implanting the second species into the source region, wherein a diffusion of the boron and arsenic species results thereby.

Claim 22 (New): The method of claim 21 wherein said hard bake comprises heating said patterned photoresist layer to a temperature between 75° C and 200° C.

Claim 23 (New): The method of claim 21 wherein the first implantation energy and dose comprises an energy of about 300KeV to about 500KeV and a dose of about 5xE13cm-2 to about 5xE14cm-2.

Claim 24 (New): The method of claim 21 wherein the second implantation energy and dose comprises an energy of about 40KeV to about 60KeV and a dose of about 5xE12cm-2 to about 5xE13cm-2.

Claim 25 (New): The method of claim 21 wherein said thermal annealing cycle occurs at a temperature between 800° C and 1200° C.

Claim 26 (New): The method of claim 21 further comprising forming a gate dielectric layer overlying the deep n-well region.